CLAIMS

Please withdraw claims 6-16 from consideration and enter new claims 22-32.

1. (Original) A data communications system including a bidirectional buffer coupled among a transmitter, a receiver, and a transmission line, wherein the bidirectional buffer comprises an output differential amplifier section that generates an output logic signal from positive polarity data signals and negative polarity data signals received from the transmitter and the transmission line, wherein the output logic signal represents data received on the transmission line, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate with a higher logic threshold voltage than a mid-supply voltage of the output differential amplifier section, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a ground path of the at least one logic gate.

2. (Original) A bidirectional bridge circuit for interfacing between a transmission line and a communication device, the bidirectional bridge circuit comprising an output differential amplifier coupled to receive inputs including positive polarity data signals and negative polarity data signals and generate an output logic signal representative of data received via the transmission line, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a threshold voltage that differs from a mid-supply voltage of the output differential amplifier.

3. (Original) The bridge circuit of claim 2, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a higher input threshold voltage than a mid-supply voltage of the output differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a ground path of the at least one logic gate.

4. (Original) The bridge circuit of claim 2, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a lower input threshold voltage than a mid-supply voltage of the output differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a supply path of the at least one logic gate.

5. (Original) The bridge circuit of claim 2, wherein the output differential amplifier comprises a NAND logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NAND logic gate is higher than a mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

6. (Withdrawn) A logic gate having a threshold voltage that differs from a mid-supply voltage level, comprising a diode-connected metal-oxide-semiconductor field effect transistor (MOSFET) in a component path of the logic gate to control a threshold voltage level, wherein symmetry is controlled in switching transients of output logic signals of the logic gate.

7. (Withdrawn) The logic gate of claim 6, wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is an n-type MOSFET placed in a ground path of the logic gate, wherein the threshold voltage level is higher than the mid-supply voltage level.

8. (Withdrawn) The logic gate of claim 6, wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is a p-type MOSFET placed in a supply voltage path of the logic gate, wherein the threshold voltage level is lower than the mid-supply voltage level.

9. (Withdrawn) The logic gate of claim 6, wherein the logic gate is a NOR gate, wherein the diode-connected MOSFET is an n-type MOSFET placed in a ground path of the logic gate, wherein the threshold voltage level is higher than the mid-supply voltage level.

10. (Withdrawn) The logic gate of claim 6, wherein the logic gate is a NOR gate, wherein the diode-connected MOSFET is a p-type MOSFET placed in a supply voltage path of the logic gate, wherein the threshold voltage level is lower than the mid-supply voltage level.

11. (Withdrawn) A logic circuit including at least one logic gate, wherein the at least one logic gate includes a diode connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path of components, wherein the diode-connected MOSFET raises an input threshold voltage of the at least one logic

gate above a mid-supply voltage, wherein symmetry is controlled in switching transients of output signals of the at least one logic gate.

12. (Withdrawn) The logic circuit of claim 11, wherein the at least one logic gate comprises a NAND logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NAND logic gate is higher than the mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

13. (Withdrawn) The logic circuit of claim 11, wherein the at least one logic gate comprises a NOR logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NOR logic gate is higher than the mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

14. (Withdrawn) A logic circuit including at least one logic gate, wherein the at least one logic gate includes a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a supply voltage path of components, wherein the diode-connected MOSFET lowers an input threshold voltage of the at least one logic gate below a mid-supply voltage, wherein symmetry is controlled in switching transients of output signals of the at least one logic gate.

15. (Withdrawn) The logic circuit of claim 14, wherein the at least one logic gate comprises a NAND logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in the supply voltage path,

wherein an input threshold voltage of the NAND logic gate is lower than the mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

16. (Withdrawn) The logic circuit of claim 14, wherein the at least one logic gate comprises a NOR logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a supply voltage path, wherein an input threshold voltage of the NOR logic gate is lower than the mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

17. (Original) A method for providing a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line, the method comprising:

receiving differential pairs of signals from the transmission line and the transmitter;

generating an output logic signal to the receiver; and

controlling symmetry in switching transients of the output logic signal by increasing a logic threshold voltage of a logic gate of an output amplifier above a mid-supply voltage of the logic gate.

18. (Original) A bidirectional communications system comprising:

at least one transmitter;

at least one receiver; and

at least one buffer coupling the at least one transmitter and the at least one receiver to at least one transmission line, the at least one buffer comprising:

at least one amplifier that amplifies and combines corresponding positive and negative polarity data signals from the at least one transmitter and the at least one transmission line to generate single-ended output logic signals representative of data received on the transmission line, wherein the output logic signals are provided to the receiver; and

at least one transistor that controls symmetry in switching transients of the output logic signals by increasing a logic threshold voltage of a logic gate of the at least one amplifier above a mid-supply voltage of the logic gate.

19. (Original) At least one semiconductor chip having a bidirectional bridge connecting each of a transmitter and a receiver to a transmission line, wherein the bidirectional bridge comprises:

an output differential amplifier coupled to receive inputs via the transmitter and the transmission line including positive polarity data signals and negative polarity data signals and generate output logic signals to the receiver representative of data received on the transmission line, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate, wherein the at least one logic gate includes a diode-connected metal-oxide-semiconductor field effect transistor (MOSFET) in a ground path, wherein the diode-connected MOSFET raises the input threshold voltage of the at least one logic gate above a mid-supply voltage.

20. (Original) A computer-readable medium including executable instructions, which when executed in a processing system, provide a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line by:

receiving differential pairs of signals from the transmission line and the transmitter;

generating output logic signals to the receiver; and

controlling symmetry in switching transients of the output logic signals by increasing a logic threshold voltage of a logic gate of an output amplifier above a mid-supply voltage of the logic gate.

21. (Original) A bidirectional communication link, comprising:

means for receiving differential signal pairs from transmission lines and transmitters;

means for generating an output logic signal from the differential data signal pairs, wherein the output logic signal represents data received in the transmission line differential signal pairs;

means for controlling symmetry in switching transients of the output logic signal by increasing a logic threshold voltage of a logic gate of the means for generating an output logic signal above a mid-supply voltage using a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path; and

means for coupling the output logic signal to a receiver.

22. (New) A bi-directional bridge circuit comprising:

a first amplifier with an input coupled to a signal source and an output coupled to a transmission line;

a second amplifier with an input coupled to the signal source and an output coupled to a common mode feedback differential amplifier;

the common mode feedback differential amplifier with a first input coupled to the output of the second amplifier, a second input coupled to the transmission line and an output coupled to an asymmetric differential amplifier; and

the asymmetric differential amplifier with an input coupled to the output of the common mode feedback differential amplifier and an output coupled to an outgoing signal line.

23. (New) The bi-directional bridge circuit as recited in claim 22 wherein the common mode feedback differential amplifier further comprises:

a differential amplifier with a first input coupled to the output of the second amplifier, a second input coupled to the transmission line, a third input coupled to an output of a common mode feed back circuitry and an output coupled to an input of the asymmetric differential amplifier; and

the common mode feed back circuitry with a first input coupled to the output of the second amplifier, a second input coupled to the transmission line and the output coupled to the third input of the differential amplifier.

24. (New) The bi-directional bridge circuit as recited in claim 22 wherein the asymmetric differential amplifier generates an output logic signal representative

of data received via the transmission line wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a threshold voltage that differs from a mid-supply voltage of the asymmetric differential amplifier.

25. (New) The bi-directional bridge circuit as recited in claim 24 wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a higher input threshold voltage than a mid-supply voltage of the asymmetric differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a ground path of the at least one logic gate.

26. (New) The bi-directional bridge circuit as recited in claim 24 wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a lower input threshold voltage than a mid-supply voltage of the asymmetric differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a supply path of the at least one logic gate.

27. (New) The bi-directional bridge circuit as recited in claim 24 wherein the asymmetric differential amplifier comprises a NAND logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NAND logic gate is higher than a mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

28. (New) The bi-directional bridge circuit as recited in claim 24 wherein the logic gate having a threshold voltage that differs from a mid-supply voltage level, comprising a diode-connected metal-oxide-semiconductor field effect transistor (MOSFET) in a component path of the logic gate to control a threshold voltage level, wherein symmetry is controlled in switching transients of output logic signals of the logic gate.

29. (New) The bi-directional bridge circuit as recited in claim 29 wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is an n-type MOSFET placed in a ground path of the logic gate, wherein the threshold voltage level is higher than the mid-supply voltage level.

30. (New) The bi-directional bridge circuit as recited in claim 29 wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is a p-type MOSFET placed in a supply voltage path of the logic gate, wherein the threshold voltage level is lower than the mid-supply voltage level.

31. (New) The bi-directional communication link as recited in claim 21 wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is an n-type MOSFET placed in a ground path of the logic gate, wherein the threshold voltage level is higher than the mid-supply voltage level.

32. (New) The bi-directional communication link as recited in claim 21 wherein the logic gate is a NAND gate, wherein the diode-connected MOSFET is a p-type

MOSFET placed in a supply voltage path of the logic gate, wherein the threshold voltage level is lower than the mid-supply voltage level